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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,149	02/27/2002	Joseph Winkles	95-520	6606
20736 7590 06/06/2007 MANELLI DENISON & SELTER 2000 M STREET NW SUITE 700 WASHINGTON, DC 20036-3307			EXAMINER WONG, WARNER	
			ART UNIT 2616	PAPER NUMBER
			MAIL DATE 06/06/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/083,149	WINKLES ET AL.	
	Examiner	Art Unit	
	Warner Wong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 1 and 6 are objected to because of the following informalities: the claim comprises the limitation(s) "configured for". Language such as "configured for" and "adapted to" suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. See MPEP§ 2111.04. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by McConnell (US 6,988,161).

Regarding claims 1 and 6, McConnell describes a method/channel adapter (fig. 2, Infiniband network with channel adapters matching applicant's fig. 1), the method comprising:

receiving a link management packet from a link partner and in response selecting, according to InfiniBand protocol, a selected active link width [and memory for

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storing port configuration settings] (col. 10, lines 16-64, using unique Management Datagram (MAD) along with Subnet Management Packets (SMP) to select and set port configuration to memory such as the Active Link Width);

[link layer module with bus controller for] setting a multiplexer circuit, configured for selectively switching frame data of a prescribed maximum link width to a selected one of a plurality of available link widths, to the selected active link width (fig. 5-6 & col. 10, lines 16-64, selecting port's Active Link Width to either 1x, 4x or 12x, where the end node's port performs multiplexing means for combining packets of VL 0-15 as shown in fig. 6);

receiving the frame data from an output buffer according to the prescribed maximum link width (fig. 6 & col. 9, line 56 to col. 10, line 5, receiving data packets 310 (frame data) from receive VL's FIFO (output) buffers according to the set (maximum) Active Link Width);

outputting the frame data from the multiplexer circuit to a transmit bus according to the selected active link width (col. 9, line 56-62, transmitting data packets 310 from the multiplexing means of fig. 6 according to the set Active Link Width);

Regarding claims 2 and 7, McConnell describes that the multiplexer circuit includes a first multiplexer for outputting the frame data onto a first output according to a first of the available link widths, and a second multiplexer circuit configured for switching the frame data onto a second output according to a second of the available link widths, the setting step including selecting one of the output buffer, the first output, and the second output for transfer of the frame data according to the selected active link

Width (fig. 6, multiplexing means (circuit) which can (first) multiplexes a number of VLs holding packet data 310 (frame data) as a first output when set to a (first) link width, and can (second) multiplexes a different number of VLs holding packet data 310 (frame data) as a second output when set to another (second) selected link width, where setting up the Active Link Width to 1x, 4x or 12x determines the number of supported subsets (or all) of VLs carrying data).

Regarding claims 3 and 8, McConnell describes a prescribed number of registers, corresponding to the prescribed maximum link width, for storing respective units of the frame data, the outputting step including outputting the frame data units in a sequence relative to the selected active link width (fig. 6 & col. 10, lines 2-5, VL FIFOs (registers) for storing data packets 310 (frame data) to be sent in 1x, 4x or 12 link width, inherently mapped in sequence to be multiplexed and transmitted).

Regarding claims 4 and 9, McConnell describes that the second multiplexer circuit is configured for grouping the frame data units into a plurality of unit groups, the outputting step including causing the second multiplexer circuit to output each of the unit groups in sequence based on the sequencing signals (fig. 6 & col. 10, lines 6-10, where the (second) multiplexing means (circuit) multiplexes (groups) data packets 310 (frame data), the step of multiplexing the subset of VLs for transmission of a link is inherently in order (sequence) based on selected VLs (sequencing signals)).

Regarding claims 5 and 10, McConnell describes that the outputting step includes outputting from the first multiplexer a corresponding one of the frame data units in sequence (fig. 6 & col. 10, lines 6-10, where the (first) multiplexing means

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(multiplexer) outputs data packets 310 (frame data) from the VL FIFOs in order (sequence)).

Response to Arguments

2. Applicant's arguments filed March 2, 2007 have been fully considered but they are not persuasive.

From p. 1, last paragraph to p.2, paragraph 1, the applicant argues that the McConnell reference fails to disclose the claim limitations "a multiplexer is configured for selectively switching frame data of a prescribed maximum link width to a selected one of a plurality of available link widths". In particular, the applicant argues that McConnell does not disclose a multiplexer. The examiner respectfully disagrees.

Firstly, claims 1 and 6 have multiple instances of the limitation "configured for", which renders the claim limitation **optional** to the subsequent descriptive action/functionality (see above claim objection).

The examiner also notes that he did not equate multiplexers 1430 and 1450 of fig. 14 to be the multiplexers in the limitations of claims 1 & 6 as argued. Regarding fig. 6 as part of the argument, the examiner reviewed the McConnell specification col. 10, lines 6-46: "According to the InfiniBand TM Architecture specification, each Port may support, but not limited thereto, up to 16 virtual lanes (VL).. The actual data VLs that a Port uses may be configured by a fabric manager 250 .. LinkWidthSupported field used to report the number of lanes supported by the Port .. Link WidthEnable field used to

control the number of lanes enabled for the port .. LinkWidthActive field used to report the number of active lanes for the Port.”

From the particular citation above describing fig. 6, the examiner concludes the one with ordinary skill in the art will interpret that the port depicted in fig. 6 combines/multiplexes virtual lanes to be transmitted. Hence, the examiner re-asserts that the McConnell reference describe the multiplexing means (multiplexer).

On p. 2, paragraph 2-4 and p. 3 paragraph 3, the applicant argues that the specification of the instant application explicitly distinguishes between virtual lanes and link width on p. 4, lines 4-11 and p. 5, lines 20-24, and concludes that the examiner's broad interpretation cannot encompass virtual lanes since it will be inconsistent with the specification. The examiner respectfully disagrees.

The examiner asserts the rejection is proper because it is based on the interpretation of claims 1 and 6 in light of the specification. The above argument from the applicant is regarded as **“reading the limitations of the specification into the claim”** which is held invalid per MPEP 2111:

“The court explained the ‘reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is quite different thing from reading limitations of the specification into a claim .. i.e. the impermissible importation of subject matter from the specification into the claim. See also In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed.Cir. 1997) (The court held that the PTO is not required, in the course of prosecution, to interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the ‘PTO

applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification.'")

In summary, the brief claims of 1 and 6 can be reasonably interpreted per the rejection unless additional claim language is amended to narrow the scope of interpretation.

On p. 3 paragraph 2, the applicant argues that multiple implementations can be used in place of a multiplexer, such as using multiple transceivers each supporting separate link width as recited in col. 14, lines 10-16 of McConnell. The examiner respectfully disagrees.

The examiner believes that the applicant misinterpreted that there is a difference between the combining/multiplexing and transmitting/receiving at the port transceiver. Clearly, the specification detailing fig. 6 & fig. 6 itself describe multiple VLs combining into a port. This is a separate aspect from how a combined signal is being transmitted/received at the port: whether to use one link transceivers or multiple separate speed transceivers as being the correct interpretation for col. 14, lines 10-16 of McConnell.

On p. 4 paragraph 2, the applicant again re-contentends that there is no multiplexer circuit (multiplexing means) or a transmit bus depicted in fig. 6. However, as explained above, fig. 6 & the respective specification details do describe combining (multiplexing) VLs to be transmitted across the physical link (transmit bus).

On p. 4, paragraph 3, the applicant similarly argues that fig. 6 of McConnell lacks multiplexer circuits (multiplexing means), which can be addressed from the response to such similar argument above regarding fig. 6.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Vajjhala (US 7,150,021) describing a method and apparatus to interconnect Infiniband devices according to resource allocation table, Gil (US 7,149,221) describing apparatus and methods for increasing bandwidth in an Infiniband switch and Rojas (US 7,209,478) describing apparatus and methods for dynamic reallocation of Virtual Lane Buffer space.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 6:30AM - 3:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Warner Wong
Examiner
Art Unit 2616

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KWANG BIN YAO
SUPERVISORY PATENT EXAMINER

